UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,416	11/16/2001	Ta-Lee Yu	B-4392 619330-6	5531

36716 7590 02/09/2006

LADAS & PARRY
5670 WILSHIRE BOULEVARD, SUITE 2100
LOS ANGELES, CA 90036-5679

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,416	YU ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4-6,13,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-3, 7-12 and 14-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support for the claimed limitation of at least one of the isolated islands being completely bordered by the first doped region, as recited in claims 1 and 12, since the at least one of the isolated islands is not bordered (has a boundary) in its lowest part by the first doped region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polgreen et al. (5,465,189) in view of Lin (5,763,919).

Regarding claims 1 and 11-12, Polgreen et al. teach in figure 8 and related text a low voltage triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit to protect core circuits of the IC from ESD event, the ESD protection circuit comprising:

a semiconductor substrate having the first conductivity type (p-type);

an well region (n well) having the second conductivity type (n-type), formed in the semiconductor substrate;

an anode doped region (p type anode) having the first conductivity type (p-type), formed in the well region (n well);

a gate structure 39, formed in the semiconductor substrate and outside the well region, the gate structure 39 having a first side and a second side;

a first doped region (n-type doped region is formed on the right side of the gate) having the second conductivity type (n-type), formed between the well region and the gate structure, immediately adjacent to the first side of the gate structure in the semiconductor substrate; and

a second doped region (n-type doped region is formed on the left side of the gate) having the second conductivity type (n-type), formed next to the second side of the gate structure in the semiconductor substrate, wherein the first doped region and the second doped region are heavily doped regions.

Polgreen et al. do not teach a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely bordered by the first doped region.
Lin teaches in figures 5c and 6c a plurality of isolated islands 54 distributed in the first doped region 60 so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely bordered by the first doped region.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely bordered by the first doped region, in Polgreen et al. device in order to evenly distribute the electric current during an ESD event. The combination is motivated by the teachings of Lin who points out the advantages of using a plurality of isolated islands distributed in the first doped region.

Regarding claims 12 and 18, prior art teaches the entire claimed structure, as applied to claim 1 above, including a semiconductor control rectifier, comprising an anode (an anode is a node portion, which is a connection between the PAD and the p-type region), a anode gate (n well), a cathode (a cathode is a node portion, which is a connection between the Vss and the n-type region) and a cathode gate (p-type substrate), the anode (an anode is a node portion, which is a connection between the PAD and the p-type region) is coupled to the pad (PAD), and a MOS having a second conductivity type

(n-type), formed on a semiconductor substrate having a first conductivity type (p-type) comprising a well (n well) having the second conductivity type (n-type).

Regarding claims 2-3, the combined device shows a first contact region (Polgreen et al.; p-type contact region) having the first conductivity type (p-type), formed in the semiconductor substrate;

a second contact region (Polgreen et al.; n-type contact region) having the second conductivity type (n-type), formed in the well region (Polgreen et al.; n well); wherein

the first contact region is coupled to the second doped region and a power pad (Polgreen et al.; Vss) of the integrated circuit, and the anode doped region is coupled to the pad, and wherein

the second contact region is coupled to the anode doped region.

Regarding claims 7-10 and 14-17, the combined device teaches isolated islands 54 are field oxide having approximately the same width, wherein each of the isolated islands is elongated and approximately parallel and perpendicular to the first side of the gate structure.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 7-12 and 14-18 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
2/3/06

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800